

Claims

We claim:

1. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;
an organic substrate having a second electrically conductive pad thereon, wherein a
surface area of the first pad exceeds a surface area of the second pad; and
a solder member electrically coupling the first pad to the second pad.

2. The electronic structure of claim 1, wherein a coefficient of thermal expansion (CTE) of the
organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

3. The electronic structure of claim 1, wherein P is between about .15 and about .75, wherein P is
defined as $(C_{\text{SOLDER}} - C_{\text{ORGANIC}})/(C_{\text{SOLDER}} - C_{\text{SEMI}})$, wherein C_{SOLDER} is a CTE of the solder member,
wherein C_{ORGANIC} is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the
semiconductor substrate.

4. The electronic structure of claim 1, wherein the organic substrate includes an organic material
selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and
combinations thereof.

1 7. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon, wherein a

4 surface area of the first pad exceeds a surface area of the second pad;

5 a solder member electrically coupling the first pad to the second pad; and

6 an underfill material between the semiconductor substrate and the organic substrate,

7 wherein the underfill material encapsulates the solder member, and wherein the underfill material

8 has an elastic modulus of at least about 1 gigapascal.

1 8. An electronic structure, comprising:

2 a semiconductor chip having a first electrically conductive pad thereon;

3 an organic chip carrier having a second electrically conductive pad thereon, wherein a

4 surface area of the first pad exceeds a surface area of the second pad;

5 a solder member electrically coupling the first pad to the second pad; and

6 an underfill material between the semiconductor chip and the organic chip carrier,

7 wherein the underfill material encapsulates the solder member, and wherein the underfill material

8 has an elastic modulus of at least about 1 gigapascal.

1 9. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon, wherein a

4 surface area of the first pad exceeds a surface area of the second pad by a factor of at least about

5 1.2; and

6 a solder member electrically coupling the first pad to the second pad.

10. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a

surface area of the first pad exceeds a surface area of the second pad by a factor between about

1.1 and about 1.3; and

a solder member electrically coupling the first pad to the second pad.

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1 12. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon; and

4 a solder member electrically coupling the first pad to the second pad, wherein a

5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6 substrate is at least about 0.25 mm.

13. The electronic structure of claim 12, wherein a coefficient of thermal expansion (CTE) of the

organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

14. The electronic structure of claim 12, wherein P is between about .15 and about .75, wherein P

is defined as $(C_{\text{SOLDER}} - C_{\text{ORGANIC}})/(C_{\text{SOLDER}} - C_{\text{SEMI}})$, wherein C_{SOLDER} is a CTE of the solder

member, wherein C_{ORGANIC} is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the

semiconductor substrate.

15. The electronic structure of claim 12, wherein the organic substrate includes an organic

material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene,

and combinations thereof.

16. The electronic structure of claim 12, wherein the solder member includes a controlled

collapse chip connection (C4) solder ball.

17. The electronic structure of claim 12, wherein the solder member includes a lead-tin alloy.

1 18. An electronic structure, comprising:

2 a semiconductor chip having a first electrically conductive pad thereon;

3 an organic chip carrier having a second electrically conductive pad thereon;

4 a solder member electrically coupling the first pad to the second pad, wherein a

5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6 substrate is at least about 0.25 mm; and

7 an underfill material between the semiconductor chip and the organic chip carrier,

8 wherein the underfill material encapsulates the solder member, and wherein the underfill material

9 has an elastic modulus of at least about 1 gigapascal.

1 19. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon;

4 a solder member electrically coupling the first pad to the second pad, wherein a

5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor

6 substrate is at least about 0.25 mm; and

7 an underfill material between the semiconductor substrate and the organic substrate,

8 wherein the underfill material encapsulates the solder member, and wherein the underfill material

9 has an elastic modulus of at least about 1 gigapascal.

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20. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a

distance from a centerline of the solder member to a closest lateral edge of the semiconductor

substrate is at least about 0.40 mm.

[illegible]

1 21. A method of forming an electronic structure, comprising:

2 forming a semiconductor substrate having a first electrically conductive pad thereon;

3 forming an organic substrate having a second electrically conductive pad thereon,

4 wherein a surface area of the first pad exceeds a surface area of the second pad; and

5 electrically coupling, by use of a solder member, the first pad to the second pad.

1 22. The method of claim 21, wherein a coefficient of thermal expansion (CTE) of the organic

2 substrate is between about 10 ppm/°C and about 18 ppm/°C.

1 23. The method of claim 21, wherein P is between about .15 and about .75, wherein P is defined

2 as $(C_{\text{SOLDER}} - C_{\text{ORGANIC}})/(C_{\text{SOLDER}} - C_{\text{SEMI}})$, wherein C_{SOLDER} is a CTE of the solder member,

3 wherein C_{ORGANIC} is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the

4 semiconductor substrate.

1 24. The method of claim 21, wherein the organic substrate includes an organic material selected

2 from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations

3 thereof.

1 25. The method of claim 21, wherein the solder member includes a controlled collapse chip

2 connection (C4) solder ball.

1 27. A method of forming an electronic structure, comprising:

2 forming a semiconductor chip having a first electrically conductive pad thereon;

3 forming an organic chip carrier having a second electrically conductive pad thereon,

4 wherein a surface area of the first pad exceeds a surface area of the second pad;

5 electrically coupling, by use of a solder member, the first pad to the second pad; and

6 placing an underfill material between the semiconductor chip and the organic chip carrier,

7 wherein the underfill material encapsulates the solder member, and wherein the underfill material

8 has an elastic modulus of at least about 1 gigapascal.

1 28. A method of forming an electronic structure, comprising:

2 forming a semiconductor substrate having a first electrically conductive pad thereon;

3 forming an organic substrate having a second electrically conductive pad thereon,

4 wherein a surface area of the first pad exceeds a surface area of the second pad;

5 electrically coupling, by use of a solder member, the first pad to the second pad; and

6 placing an underfill material between the semiconductor substrate and the organic

7 substrate, wherein the underfill material encapsulates the solder member, and wherein the

8 underfill material has an elastic modulus of at least about 1 gigapascal.

1 29. A method of forming an structure, comprising:

2 forming a semiconductor substrate having a first electrically conductive pad thereon;

3 forming an organic substrate having a second electrically conductive pad thereon,

4 wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at

5 least about 1.2; and

6 electrically coupling, by use of a solder member, the first pad to the second pad.

1 30. A method of forming an electronic structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon,
4 wherein a surface area of the first pad exceeds a surface area of the second pad by a factor
5 between about 1.1 and about 1.3; and
6 electrically coupling, by use of a solder member, the first pad to the second pad.

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31. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon,

wherein a surface area of the first pad exceeds a surface area of the second pad by a factor

between about 1.3 and about 2.0; and

electrically coupling, by use of a solder member, the first pad to the second pad.

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

1 32. A method of forming an electronic structure, comprising:

2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon; and
4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein
5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm.

1 33. The method of claim 32, wherein a coefficient of thermal expansion (CTE) of the organic
2 substrate is between about 10 ppm/°C and about 18 ppm/°C.

1 34. The method of claim 32, wherein P is between about .15 and about .75, wherein P is defined
2 as $(C_{\text{SOLDER}} - C_{\text{ORGANIC}})/(C_{\text{SOLDER}} - C_{\text{SEMI}})$, wherein C_{SOLDER} is a CTE of the solder member,
3 wherein C_{ORGANIC} is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the
4 semiconductor substrate.

1 35. The method of claim 32, wherein the organic substrate includes an organic material selected
2 from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations
3 thereof.

1 36. The method of claim 32, wherein the solder member includes a controlled collapse chip
2 connection (C4) solder ball.

1 37. The method of claim 32, wherein the solder member includes a lead-tin alloy.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

1 38. A method of forming an electronic structure, comprising:

2 forming a semiconductor chip having a first electrically conductive pad thereon;

3 forming an organic chip carrier having a second electrically conductive pad thereon;

4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein
5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm; and

7 placing an underfill material between the semiconductor chip and the organic chip carrier,
8 wherein the underfill material encapsulates the solder member, and wherein the underfill material
9 has an elastic modulus of at least about 1 gigapascal.

1 39. A method of forming an electronic structure, comprising:

2 forming a semiconductor substrate having a first electrically conductive pad thereon;

3 forming an organic substrate having a second electrically conductive pad thereon;

4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein
5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm; and

7 placing an underfill material between the semiconductor substrate and the organic
8 substrate, wherein the underfill material encapsulates the solder member, and wherein the
9 underfill material has an elastic modulus of at least about 1 gigapascal.

